Dr. Soumya Pandit

Assistant Professor, Stage-III,
Institute of Radio Physics and Electronics,
University of Calcutta,
and
Chartered Engineer [India],
Electronics and Telecommunication Engineering

Personal Information

- Date of Birth: 09.07.1976
- Gender Male
- Residential Address 168, Rajdanga School Road
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Contact Details

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  University of Calcutta
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  soumya.pandit.rpe@gmail.com

Academic Details

- 2009 Ph.D. in Engineering, Indian Institute of Technology, Kharagpur
- 2002 M.Tech in Radio Physics and Electronics, University of Calcutta

- 2000 M.Sc in Electronic Science, University of Calcutta
- 1998 B.Sc with Honours in Physics, University of Calcutta

Employment Details

- 2017 (Feb)-onwards Assistant Professor, Stage-III
  Institute of Radio Physics and Electronics
  University of Calcutta

- 2012 (Feb)-2017 (Feb) Assistant Professor, Stage-II
  Institute of Radio Physics and Electronics
  University of Calcutta

- 2008 (Nov)- 2012 (Feb) Assistant Professor, Stage-I
  Institute of Radio Physics and Electronics
  University of Calcutta

- 2008 (Feb)-2008 (Oct) Assistant Professor
  Electronics and Communication Engineering Department
  Meghnad Saha Institute of Technology

- 2003 (Aug)-2008 (April) Research Consultant
  Advanced VLSI Design Laboratory
  SRIC, IIT Kharagpur

- 2002 (Jan)-2003 (July) Lecturer
  Electronics and Communication Engineering Department
  Meghnad Saha Institute of Technology

Academic Responsibilities

- Undergraduate and postgraduate level teaching (theory and laboratory) as per University of Calcutta curriculum at Institute of Radio Physics and Electronics, 2008 (Nov-onwards)
- Teacher –In Charge of IC Design Laboratory, a research and post-graduate level teaching laboratory.
- Teacher-In Charge (jointly) of Electronic Circuits Laboratory and Analog Circuits Simulation, under graduate level teaching laboratories.
- Member of the Syllabus sub-committee responsible for up gradation of B.Tech syllabus in Electronics and Communication Engineering at the Institute of Radio Physics and Electronics
- Member of the Syllabus sub-committee responsible for upgradation of M.Tech VLSI Design syllabus.

- Member of the Board of Studies in Electronics and Communication Engineering and Board of Post Graduate Studies in VLSI Design
- Coordinator of the 3rd Semester B.Tech course in Electronics and Communication Engineering.
- Member of Admission and Selection Committee for M.Tech students admission.
- Member of the Departmental Committee.

Research Interest

- Compact Modeling of Semiconductor Devices
- Ultra-Low Power Design of CMOS Analog ICs.
- Design for Manufacturability for CMOS ICs

Professional Memberships

- Senior Member, IEEE, Membership No: 80057634
- Member, IE(I), Membership No: M-1654378
- FOSET, Life Member, Membership No: LM/2011-2104

Involvements in IEEE

- Founded the IEEE ED Student Branch University of Calcutta (SBC28561A) in the capacity of chapter advisor
- Treasurer, IEEE EDS Calcutta Chapter 2012-2013
- Chair, IEEE EDS Calcutta Chapter, 2014-2015
- Members of the Regions and Chapter Committee, IEEE Electron Devices Society, USA, 2016-2017
- Vice Chair, SRC, Region-10, IEEE Electron Devices Society, USA, 2018- present

Other Professional Achievements

- Member of the Board of Studies in Electronics and Communication Engineering, National Institute of Science and Technology, Berhampur, Autonomous College under Biju Pattanaik University of Technology, Odhisa.
- Session Chair, 5th International Conference on Opto-Electronics and Applied Optics (OPTRONIX-2019)
- Session Chair, Modeling and Simulation Track, 4th IEEE International Conference on Emerging Electronics (ICEE), 16-19 Dec, 2018
- Member of the Technical Program Committee, 31st International Conference on VLSI Design, 2018

- Member of the Technical Program Committee, 21st International Symposium on VLSI Design and4 Test, 2017, IIT Roorkee
- Member of the Technical Program Committee, 7th International Symposium on Embedded Computing and System Design, 2017, NIT Durgapur
- Ph.D. Forum Chair, 29th International Conference on VLSI Design, 2016
- Session Chair, International Conference, Microelectronics, Circuits and Systems (Micro-2014), International Conference, Microelectronics, Circuits and Systems (Micro-2014)6

Publications

Published Papers in Journals

S. No	Title with page nos.	Journal	ISSN/ISBN No	Whether peer reviewed. Impact factor, if any	No. of co-author	Whether you are the main author	API Score
1.	Performance Assessment of CMOS circuits using III-V on Insulator MOS Transistors	Silicon Springer Nature, 2020, 13 July 2020,	1876-990X	YES, IF= 1.499	1	Yes, Supervisor	
2.	A Global Routing Method for Graphene Nanoribbons Based Circuits and Interconnects	ACM Journal on Emerging Technologies in Computing Systems, Vol. 16, No. 3, May 2020	1550-4832	YES, IF=1.367	2	Yes, Supervisor	
3.	Charge-Based Compact Drain Current Modeling of InAs-OI-Si MOSFET Including Subband Energies and Band Nonparabolicity	IEEE Transactions on Electron Devices	0018-9383	YES, IF = 2.62	2	Yes, Supervisor	

4.	Analysis of scaling of thickness of the buffer layer on analog/RF and circuit performance of InAs-OI-Si MOSFET using NQS model	International Journal of Numerical Modeling, John Willey	1099-1204	YES, IF= 0.795	1	Yes, supervisor	
5.	Analysis of Drain Current Local Variability of an n-Channel EδDC MOSFET Due to RDD Considering Inversion Charge and Correlated Mobility Fluctuations	IEEE Transactions on Electron Devices,	0018-9383	YES, IF = 2.62	1	Yes	**28**
6.	Effects of BOX Engineering on Analog/RF and circuit performance of InGaAs-OI-Si MOSFET, Accepted for Publications	International Journal of Electronics, Taylor and Francis, UK	ISSN 0020-7217 (Print); ISSN 1362-3060 (Online)	Yes. IF= 0.459	1	Yes Supervisor	**21**
7.	Study of G-S/D underlap for enhanced analog performance and RF/circuit analysis of UTB InAs-OI-Si MOSFET using NQS small signal model, http://dx.doi.org/10.1016/j.spmi.2016.11.053	Superlattice and Microstructure, Elsevier, 2016.	ISSN: 0749-6036	Yes IF = 2.117	1	Yes Supervisor	**28**
8.	Study of temperature variation on threshold voltage and sub-threshold slope of EδDC MOS transistor including quantum corrections and reduction techniques, DOI 10.1007/s00542-	Microsystem Technologies, Springer, 2016,	Print ISSN 0946-7076, Online ISSN 1432-1858	Yes IF = 0.974	4	Yes Supervisor and Corresp-onding Author	**21**

	016-2995-z						
9.	Substrate Bias Effect of Epitaxial Delta Doped Channel MOS Transistor for Low Power Applications	International Journal of Electronics, Taylor and Francis, UK, Vol. 104, No 1 pp 47-63,	ISSN 0020-7217 (Print); ISSN 1362-3060 (Online)	Yes, IF= 0.459	2	Yes Supervisor and Corresp-onding Author	**21**
10.	Channel Profile Design of EδDC MOSFET for High Intrinsic Gain and Low VT Mismatch, pp 551-557	IEEE. Transaction on Electron Devices, Vol. 63, No. 2, 2016 pp 551-557 IEEE, USA,	ISSSN No: 0018-9383	YES, IF = 2.472	1	Yes Supervisor and Corresp-onding Author	**28**
11.	SarmistaSengupta and Soumya Pandit, 'Study of performance scaling of 22nm epitaxial delta-doped channel MOS transistor', pp 1-15	International Journal of Electronics	0020-7217 (Print), 1362-3060 (Online)	YES Inpact = 0.751	1	1	**21**
12.	Modeling and Design of a Nano Scale CMOS Inverter for Symmetric Switching Characteristics', VLSI Design, vol. 2012, Article ID 505983, 13 pages, 2012.	VLSI Design, vol. 2012 (2012) Indexed journal	ISSN: 1065-514X (Print) ISSN: 1563-5171 (Online) doi:10.1155/VLSI	Yes	1	Yes Corresp-onding Author	**17.5**
13.	A Methodology for Generation of Performance Models for the Sizing of Analog High-level Topologies' Article ID 475952, 17	VLSI Design, vol. 2011 (2011) Indexed journal	ISSN: 1065-514X (Print) ISSN: 1563-5171 (Online)	Yes	2	Yes Supervisor/mentor	**17.5**

	pages		doi:10.1155/VLSI				
14.	Adaptive Sampling Algorithm for ANN-based Performance Modeling of Nano-scale CMOS Inverter pp 214	Int. Journal Electrical and Electronics Engineering, WASET, USA, Vol 5, No 4, 2011 Indexed journal	ISSN: 2010-3972(Electronic) ISSN: 2010-3964 (Print)	YES	1	YES Supervisor	**17.5**
15.	'An Automated High-Level Topology Generation Procedure for Continuous-Time ΣΔ Modulator', Integration, the VLSI journal, 2010, Vol. 43 pp 289-304,	Integration-the VLSI Journal Indexed journal	0167-9260	Yes Impact factor = 1.00	2	Yes 1st Author	**24.5**
16.	A Fast Exploration Procedure for Analog High-Level Specification Translation, pp 1493 - 1497	IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, Vol 27, No 8, Aug. 2008	0278-0070	Yes Impact factor = 1.942	3	Yes 1st Author	**24.5**

Publications other than Journal Articles (books, chapters in books)

Book

S. No	**Chapter Title**	**Book title, editor and publisher**	**ISSN/ISBN No**	**No. of co-authors**	**Whether you are the main author**	**API Score**
1.	BOOK	Nano-Scale CMOS Analog Circuits: Models and CAD Techniques for High-Level Design, CRC Press, USA, Taylor & Francis, UK and others, 2014	Print ISBN: 978-1-4665-6426-8 eBook ISBN: 978-1-4665-6428-2	2	Yes. 1st Author	**21**

Book Chapters

S. No	Chapter Title	Book title, editor and publisher	ISSN/ISBN No	No. of co-authors	Whether you are the main author	API Score
1.	Design Methodology for Ultra-Low-Power CMOS Analog Circuits for ELF-SLF Applications	Nanoscale VLSI, Editors: Dr. Rohit Dhiman, Dr. Rajeevan Chandel Publisher: Springer Singapore	978-981-15-7937-0	Nil	Yes	**10**
2.	UTB III-V-OI-Si MOS Transistor: the future Transistor for VLSI Design	VLSI and Post-CMOS Electronics, Edited by R.Dhiman and R.Chandell, IET, UK.	ISBN-13: 978-1-83953-051-7	1	YES	**7**
3.	CMOS Design and Analysis of Four Quadrant Analog Multiplier Circuit for LF Applications	Kundu S., Acharya U., De C., Mukherjee S. (eds) Lecture Notes in Electrical Engineering, vol 602. Springer, Singapore. https://doi.org/10.1007/978-981-15-0829-5_28	978-981-15-0828-8	1	Yes	**7**
4.	Design of a Health Monitoring System for Heart Rate and Body Temperature Sensing Including Embedded Processing using ARM Cortex M3	Das A., Nayak J., Naik B., Pati S., Pelusi D. (eds) Computational Intelligence in Pattern Recognition. Advances in Intelligent Systems and Computing, vol 999. Springer, Singapore. https://doi.org/10.1007/978-981-13-9042-5_9	978-981-13-9041-8	3	No	**3**
5.	Variability in Nano-scale MOS	Nanoscale Devices: Physics, Modeling and	ISBN: 9781138060340	1	Yes. Supervis	**10**

	Transistor and EδDC MOS Transistor	their Application, CRC Press, USA., Editor: B.K.Kaushik, Chapter 2			or	
6.	Behavioral Modeling of Differential Inductive Seismic Sensor and Implementation of its Read Out Circuit	Communication, Devices, and Computing, Editor: JaydebBhaumikIndrajitChakrabartiBishnu Prasad De Banibrata Bag Surajit Mukherjee, Springer Lecture Notes in Electrical Engineering, Vol. 470, April 2018	ISBN 978-981-10-8585-7	4	No	**3**
7.	Nanoscale MOSFET: MOS Transistor as Basic Building Block	Introduction to Nano: Basics to Nanoscience and Nanotechnology, 2015 Publisher: Springer, Editor A.Sengupta and C.K.Sarkar.	ISBN 978-3-662-47314-6	Nil	Yes, single author	**10**
8.	Statistical Characterization of Flicker Noise Fluctuation of a Nano-Scale NMOS Transistor Page no 203-214	Advanced Nanomaterials and Nanotechnology Editor: P.K.Giri et al Publisher: Springer-Verlag Berlin Heidelberg 2013	ISBN No: 978-3-642-34215-8	1	Yes. Supervisor	**10**
9.	MOSFET Characterization for VLSI Circuit Simulation Page no: 267-362	Technology Computer Aided Design: Simulation for VLSI MOSFET Editor: Chandan Kumar Sarkar Publisher: CRC Press, USA, May 2013	ISBN No: 978-1-4665-1265-8	Nil	Yes, single author	**10**

Selected Conference Proceedings as Supervising Author

S. No	**Title with page nos.**	**Details of Conference Publications**	**ISSN/ISBN No**	**No of Co-Authors**	**Whether you are the main author**	**API Score**
1.	'Study of LER/LWR Induced VT	Accepted for Publications in the	ISBN No: 978-1-5090-4724-	1	Yes. Supervisor	**5**

	Variability of an EδDC n-channel MOS Transistor'	Proceedings of Dev IC 2017, Publisher: IEEE	6/17			
2.	'Study of Short Channel Characteristics of Gate Underlapped InGaAs-OI-Si MOS Transistor'	Proceedings of NCDC 2016, Editor: A.K.Panda, Publisher: IPM Pvt. Ltd, Odhisha	ISBN: 978-93-82208-78-5	1	Supervisor	**5**
3.	Effect of Buried Oxide (BOX) Thickness Scaling on Analog/RF Performance of InGaAs-on-Insulator MOS Transistor	Proceedings of 2nd Int. Conf. Microelectronics, Circuits and Systems, organized by IASTM, Editor: D.Acharya, Publisher: Arisha Creation, Kolkata	ISBN: 81-85824-46-0	1	Supervisor	**5**
4.	Temperature Analysis of Threshold Voltage and Sub-threshold slope of Epitaxial Delta Doped Channel MOS Transistor for SoC Applications, Pp105-109, 2015	Proceedings of 2nd Int. Conf. Microelectronics, Circuits and Systems, organized by IASTM, Editor: D.Acharya Publisher: Arisha Creation, Kolkata	ISBN: 81-85824-46-0	1	Supervisor	**5**
5.	Amino acid classification based on Electrical response of its Codon composition	Proceedings of IEEE Int. Conference on Research in Computational Intelligence and Communication Networks, Pp279-284, 2015	Electronic ISBN: 978-1-4673-6735-6 CD-ROM ISBN: 978-1-4673-6734-9	2	2nd Author	**4**
6.	Study of Wide Temperature Variation (100-500 K) on Drain Current Characteristics of a 22nm n-channel EδDC MOS Transistor	Proceedings of 4th International. Conference on Computing, Communication and Sensor Network, 2015, organized by IASTM, Editor: D.Acharya, Publisher: IASTM	ISBN: 81-85824-46-0	1	Supervisor	**5**

7.	Impact of Gate Underlap on Analog/RF Performance of InGaAs-OI-Si Substrate MOS Transistor for SoC Computing Applications	Proceedings of 4th International. Conference on Computing, Communication and Sensor Network 2015, organized by IASTM, Publisher: IASTM	ISBN: 81-85824-46-0	1	Supervisor	**5**
8.	Study of Analog and RF Performance of UTB-OI-Si Substrate MOS Transistor using Buffered InGaAs and Silicon Channel	Proceedings of 6th International Conference CODEC 2015, Publisher: IEEE	Electronic ISBN: 978-1-4673-9513-7 CD-ROM ISBN: 978-1-4673-9511-3 Print on Demand(PoD) ISBN: 978-1-4673-9514-4	1	Supervisor	**5**
9.	Power Aware Clustering and Placement for FPGAs	1st International Science and Technology Congress, IEMCON 2014, Publisher: Elsevier	ISBN: 9789351072485	3	Supervisor	**6**
10.	Study of Reverse Substrate Bias Effect of 22nm node Epitaxial Delta Doped Channel MOS Transistor	VLSI Design and Test, 18th International Symposium on, Publisher: IEEE	Electronic ISBN: 978-1-4799-4006-6 Print ISBN: 978-1-4799-5088-1 CD-ROM ISBN: 978-1-4799-4007-3	1	Supervisor	**5**
11.	Threshold Voltage Modeling of Deeply Depleted Channel MOSFET and Simulation Study of its Analog Performances	Electronics, Communication and Instrumentation (ICECI), 2014 International Conference, Publisher: IEEE	Electronic ISBN: 978-1-4799-3983-1 CD-ROM ISBN: 978-1-4799-3982-4	1	Supervisor	**5**
12.	An Improved gm/ID	Manoj Singh Gaur Mark Zwolinski	ISSN 1865-0929 e-ISSN	2	Supervisor	6

	Methodology for Ultra-Low-Power Nano-Scale CMOS OTA Design	Vijay Laxmi Dharmendra Boolchandani Virendra Singh Adit D. Singh (Eds.), CCIS 382, pp. 128–137, 2013. Publisher: Springer-Verlag Berlin Heidelberg 2013	1865-0937 ISBN 978-3-642-42023-8 e-ISBN 978-3-642-42024-5 DOI 10.1007/978-3-642-42024-5			
13.	Semi-Analytical Estimation of Intra-Die Variations of Analog Performances of Nano-scale NMOS Transistor pp 854904-1-5.	16th IWPSD, Proceedings SPIE edited by Y N. Mohapatra, B. Mazhari, M. Katiyar, Vol. 8549 (SPIE, Bellingham, WA, 2012)	ISSN: 0277-786X ISBN: 9780819493002	1	Supervisor	**5**

Ongoing and Completed Research Projects and Consultancies

S.No	Title	Agency	Period	Grant/Amount Mobilized (Rs. Lakh)	API
1.	Special Manpower Development Programme-Chip to Systems Design in VLSI Design	MeitY, Govt. of India	2015-	Rs. 95.09 Lakh + EDA tools and Servers procured centrally	**20**
2.	Modern Biology and Signal Processing Group,	University with Potential for Excellence, Calcutta University	2017-	Rs. 4.5 Lakh	**10**
3.	Development of a design automation tool for nano CMOS analog circuits	DST, Govt. of India	2010-2013	Rs. 12,12,000/-	**10**
4.	Device-Circuit Co-design and Integration of Device CAD and Circuit CAD for the study of	TEQIP, Phase-II, University of	Novemb er 2013-Novemb	Rs. 1 Lakh	**10**

	Nano-scale MOS Transistors for Low Power SoC Applications	Calcutta	er 2015		
5.	Statistical Modeling, Design and Optimization of Nano-CMOS Analog/RF Circuits	CRNN, University of Calcutta	2009-2011	Rs. 2 Lakh + Salary of 1 SRF	**10**

Research Guidance

(i) M.Phill/M.tech

Number	**Thesis Submitted**			**Degree Awarded**	**API Score**
22	S.No	Name of Student	Thesis Title		
	1.	SarojMondal	E123_Core Micro-Architecture	YES 2009	**5**
	2.	Sipra Mandal	Modeling, Simulation and Design of a Nano-scale CMOS Circuits using Soft Computing Techniques	YES 2010	**5**
	3.	Chandan Mukherjee	Statistical Study of the Variation of Process Parameters on the Performance of CMOS VCO and OPAMP Circuits	YES 2010	**5**
	4.	KaustavDasgupta	Design and Study of Digital Phase Locked Loop using nanoscale CMOS Technology	YES 2010	**5**
	5.	KrishnenduDey	Design of a Wide-band, Low-Power Digital Phase Locked Loop using 32-nm CMOS Technology	YES 2010	**5**
	6.	DipankarDhabak	Performance Modeling of Nano-scale CMOS Logic Circuits using Soft Computing Techniques	YES 2011	**5**
	7.	Joyjit Mukherjee	Design of a Nano-scale CMOS Inverter Circuits using Soft Computing Techniques	YES 2011	**5**

	8.	Debabrata Bose	Design of a nano-scale CMOS Inverter using Generic Algorithm.	YES 2011	**5**
	9.	SomnathPaul	Design of Amplifier for Ultra-Low Power Analog Application using nano-scale MOS Transistors	YES 2012	**5**
	10.	Abhijit Dana	SPICE Modeling and Parameter Extraction of Nano-scale MOS Transistors for Low Power Analog Circuit Applications	YES 2012	**5**
	11.	Pranjal Barman	Statistical Study of Random Discrete Dopant Effect in Scaled MOS Transistor and Its Reduction by Channel Engineering Approach.		**5**
	12.	Kritanjali Das	Study of Analog Performances of Nano-scale MOS Transistors		**5**
	13.	DebayanBairagi	Study of Substrate Bias Effect for Epitaxial Delta Doped Channel MOS Transistor	YES 2014	**5**
	14.	Aparna Das	Study of Power Aware Clustering for FPGA	YES 2014	**5**
	15.	Mousumi Ghosh	Study of Power Aware Placement for FPGA	YES 2014	**5**
	16.	Rahul Kumar Shaw	Design of a Low Power Front End OTA and PSO Application for the Optimization of Threshold Voltage Parameter of EδDC Transistor	Yes 2016	**5**
	17.	Rinkee Das	Temperature Characterization over Wide Range (100-500K) of an n-channel EδDC MOS Transistor	Yes 2016	**5**
	18.	Saswata Chatterjee	Design of a Low Frequency, Low Power, Fast Locking Digital Phase Locked Loop using SCL 180 nm technology	Yes 2017	**5**
	19.	Suman	Adaptive Noise Cancellation of Seismic	Yes	**5**

		Goswami	Signal using Least Mean Square Algorithm and Implementation using FPGA	2017	
	20.	Kaushik Sen	Modeling of a Differential Inductive Seismic Sensor and its Simulation using COMSOL Multiphysics	Yes 2017	**5**
	21.	Monalisa Dutta	Design and Implementation of FPGA Based Earthquake Early Warning System	YES 2017	**5**
	22.	Sirsha Guha	Temperature Analysis of Device Performance of a sub-50nm p-Channel SOI FinFET	YES 2019	**5**
	23.	Srabanti Saha	DC-DC Power Bulk Converter jointly with Sankalp Semiconductor as intern.	YES 2020	**5**

(ii) Ph.D Scholars

Sr. No	**Name of the Ph.D. Student**	**Registration/Enrollment Number**	**Topic of Thesis**	**Publications Made**
1.	Mrs. Sarmista Sengupta	5001 Ph.D. (tech).Proceed/11 5000 Submitted	Study of Process Variability Effects on EδDC MOS Transistor for Low Power VLSI Applications	4 Journal SCI indexed journal and several conference papers
2.	Mr. Subir Maity	Ph.D./Admission/RPE/29/2014 5000 Submitted	Study of Device and Circuit Performance of III-V-OI-Si MOS Transistor	4 SCI Indexed journal papers and several conference papers
3.	Mr. Subrata Das	Enrolled	Studies on Physical Design of VLSI Circuits based on Graphene Nanoribbon	1 SCI journal and 1 conference papers

Fellowships, Awards and Invited lectures delivered in conferences / seminars.

Award

Sr. No	**Award Name**	**Academic Body**	**Whether international/national**	**API Score**
1.	Best Paper Award for the Paper A	Noorul Islam	National	10

	Methodology for Sizing of Analog High Level Topologies using Computational Intelligence Technique	University		

Invited Lectures/Papers presented

S. No	Title of Lecture/Academic Session	Title of Conference/Seminar etc	Organized by	Whether international/national	API Score
1.	Variability in MOS Transistors	3rd International Conference on Devices and Circuits, March 2019	Kalyani Govt. Engineering College	International	**7**
2.	Unified Model for Drain Current Local Variability in MOS Transistors	4th IEEE International Conference on Emerging Electronics, 16-19th December 2018, Bangalore, India	IEEE Electron Devices Society	International	**7**
3.	Process Variability Modeling and Low Leakage Device Design in IoT Design Space"	IEEE EDS Technical Talk, Monday, 25th June 2018	Electrical Engineering Department, IIT Kanpur	National	**5**
4.	Tutorial on CMOS Analog IC Design	2 day Workshop on Emerging VLSI Techologies	Assam University, Silchar	National	**5**
5.	Invited Talk:Epitaxial Delta Doped Channel MOS Transistor: A Candidate for Smart Mobile SoC Applications	2nd International Conference on Microelectronics, Circuit and Systems, July 11, 2105	International Association of Science, Technology and Management,	International	**7**
6.	Invited Talk: Advanced MOS Transistor for Mobile SoC Design,	International Workshop on Advanced Electron Devices and Circuits,	IEEE EDS Calcutta Chapter and School of Electronics Engineering, KIIT University, 3rd-4th December 2014.	International	**7**
7.	Invited Talk: Short	1day Workshop on	Abacus Institute of	National	**5**

	Channel Effects in MOS Transistors	Advanced Semiconductor Device Modeling and Fabrication	Engineering and Management, 15th November 2014.		
8.	Keynote Talk: Nano-scale CMOS Analog Circuits: Essential Challenges and Design Methodologies,	International Conference, Microelectronics, Circuits and Systems (Micro-2014)	International Association of Science, Technology and Management, Puroshottam Institute of Engineering and Technology, Rourkela, Odisha and IETE, Kolkata. 11th July 2014.	Internati onal	**7**
9.	Session Chair	International Conference, Microelectronics, Circuits and Systems (Micro-2014)	International Association of Science, Technology and Management, Puroshottam Institute of Engineering and Technology, Rourkela, Odisha and IETE, Kolkata. 11th July 2014.	Internati onal	**7**
10.	Invited Talk: *Electron System Design and Manufacturing*	Seminar on Embedded System and VLSI	Elitte Institute of Engineering and Management, 29th March 2014	National	**5**
11.	Joint Course Director, Winter School	UGC-NRCPS Sponsored Winter School Physics and Technology of Sensors (PHYTSENS-12)	University of Calcutta 26th November 2012	National	**5**
12.	*MEMS Capacitive Sensors*	UGC-NRCPS Sponsored Winter School Physics and Technology of Sensors (PHYTSENS-12)	University of Calcutta 26th November 2012	National	**5**
13.	*Interface Electronics for Smart Sensors*	UGC-NRCPS Sponsored Winter School Physics and Technology of Sensors (PHYTSENS-12)	University of Calcutta 22nd November 2012	National	**5**
14.	*MOSFET Characterization for VLSI Circuit Simulation*	Faculty Development Program on Recent Trends on VLSI Design and Embedded Systems	C.V.Raman College of University, BPUT, Orissa 27th July 2012	National	**5**

15.	Device Characterization for VLSI Circuit Simulation	UGC-NRCPS Sponsored summer school Nano Mastd 2012,	University of Calcutta 1st June 2012	National	**5**
16.	CMOS Analog Circuits	UGC-NRCPS Sponsored summer school Techniques for Design, Fabrication and Computation of Integrated Circuits (TECHNOMICS-12)	University of Calcutta 29th May 2012	National	**5**
17.	Low Power CMOS Circuits	----------do----------	-----do---------	National	**5**
18.	Performance Modeling, Parameter Extraction Technique and Statistical Modeling of Nano-scale CMOS Transistors for VLSI Circuit Simulation	International Workshop on Device Modeling of Microsystems	MOS-AK/GSA and INAE during March 16-18, 2012 at JIIT, Noida	Internati onal	**7**
19.	Low Power CMOS Circuits	'Advances in Photonic, Electronic and Communication Systems (APECS-2012)'	Tezpur University, Date: January 24th 2012	National	**5**
20.	Parameter Extraction Technique for MOS Modeling	Advances in Electronics, Communication and Information Technology	Mizoram University Date: March 25th 2011	National	**5**
21.	Low power CMOS Design: Sources and Minimization Techniques	Advances in Electronics, Communication and Information Technology	Mizoram University, Date: March 24th 2011	National	**5**
22.	Performance Modeling of Nano Scale CMOS Inverter Circuit	International Conference on Nanotechnology and Biosensor (ICNB2-	Raghu Engineering College, Visakhapatnam (A.P), India	Internati onal	**5**

	using Least Squares Support Vector Machine	2011)			
23.	Effects of Intra-Die Process Variations on Nano-Scale CMOS Analog Circuit Performance	International Conference on Nanotechnology and Biosensor (ICNB2-2011)	Raghu Engineering College, Visakhapatnam (A.P), India	Internati onal	**5**
24	Statistical Modeling of Process Variability Effects on Nano-scale CMOS Analog and RF Circuits	IEEE Technical Talk	IEEE Calcutta Section, EDS Chapter, 22nd June 2010	National	**5**
25.	CAD for Nano CMOS Analog Design	Frontiers of Electronics and Communication	North Eastern Regional Institute of Science and Technology (NERIST), Nirjuli, Arunachal Pradesh, 8th September 2009	National	**5**
26.	CMOS Device Modeling for Analog and Digital Circuits	Summer School NanoDev 3rd June 2009	UGC-NRCPS, IRPE	National	**5**